LeCroy

QualiPHY™
Compliance Test Software

QPHY-HDMI
HDMI Serial Data
Operator's Manual

Revision A – November, 2008

Relating to the Following Release Versions:

- **Software Option Rev. 5.7**
- **HDMI Script Rev. 1.2**
- **Style Sheet Rev. 1.2**

LeCroy Corporation

700 Chestnut Ridge Road
Chestnut Ridge, NY 10977–6499
Tel: (845) 578 6020, Fax: (845) 578 5985

Internet: www.lecroy.com

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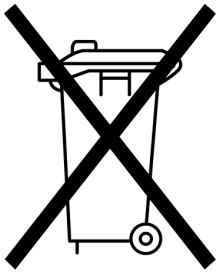

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For more information about proper disposal and recycling of your LeCroy product, please visit www.lecroy.com/recycle.

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INTRODUCTION TO QPHY-HDMI

QPHY-HDMI is an automated test package performing all of the real time oscilloscope tests for sources in accordance with version 1.3c of the High Definition Multimedia Interface Compliance Test Specification. The software can be run on LeCroy's SDA 760Zi, DDA 760Zi, WavePro 760Zi (with the SDA II option), and SDA 6020.

Required equipment

- SDA 760Zi, DDA 760Zi, WavePro 760Zi (with the SDA II option) or SDA 6020 Oscilloscope
- 8 SMA Male to SMA Male Cables
- 4 TF-HDMI-3.3V Test Adapters
- HDMI Test Fixture (as follows)

HDMI Compliance Test Fixtures

LeCroy recommends using the Efficere ET-HDMI-TPA-P (plug test adapter) used in conjunction with ET-HDMI-TPA-E (EDID board with EEPROM), as well as 8 two inch GPPO-to-SMA cables. This equipment is available from Efficere individually or as part of the ET-HDMI-TPA-S Test Adapter Set.

The ET-HDMI-TPA-S test adapter set provides a very high bandwidth, low noise evaluation vehicle that enables high-performance characterization of both plug and receptacle HDMI™ devices with bandwidth greatly exceeding the 340 MHz (10.2 Gbps) of the latest v1.3 HDMI specification

Note: The above text was taken from the ET-HDMI-TPA-S datasheet that can be found at www.efficere.com

USING QUALIPHY HDMI

QualiPHY HDMI guides the user, step-by-step, through each of the source tests described in version 1.3c of the High Definition Multimedia Interface Compliance Test Specification. To do this, the user must setup a test session.

Users choose the test configuration they wish to run. There are seven pre-loaded test configurations. They are:

- **All tests, ordered by indexed (Default)**
- **All Data Inter-Pair Skew tests**
- **Clock & Data0 tests at 74.25MHz**
- **Clock & Data0 tests at all frequencies**
- **Demo of All tests, ordered by indexes**
- **Empty Template**
- **Test 7-9 & 7-10 at all frequencies**

These pre-loaded configurations provide quick and easy ways to begin compliance testing. If the user does not want to run any of these configurations, they can create their own custom configuration (see the following section entitled Error! Reference source not found. for details). The **Empty Template** is a blank configuration meant to serve as an easy way to create your own custom configuration.

The variables are pre-loaded with the standard settings for compliance testing; however, the user may choose to create their own configuration with the variables set as desired.

QualiPHY™

QUALIPHY COMPLIANCE TEST PLATFORM

QualiPHY is LeCroy's compliance test framework which leads the user through the compliance tests. QualiPHY displays connection diagrams to ensure tests run properly, automates the oscilloscope setup, and generates complete, detailed reports.

The QualiPHY software application automates the test and report generation.

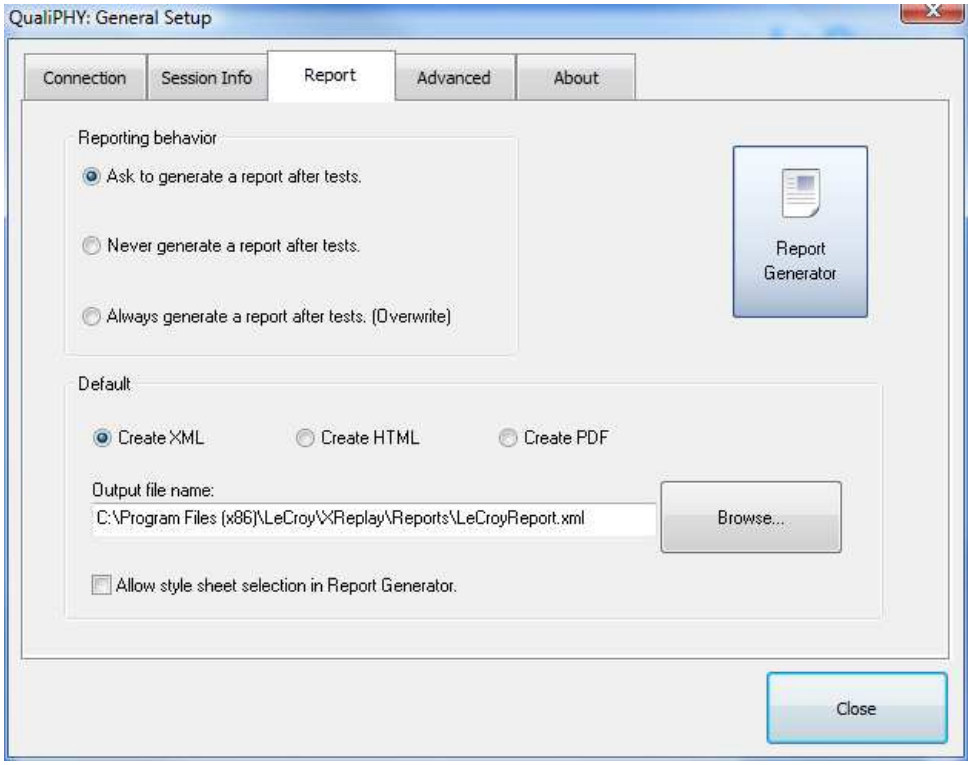
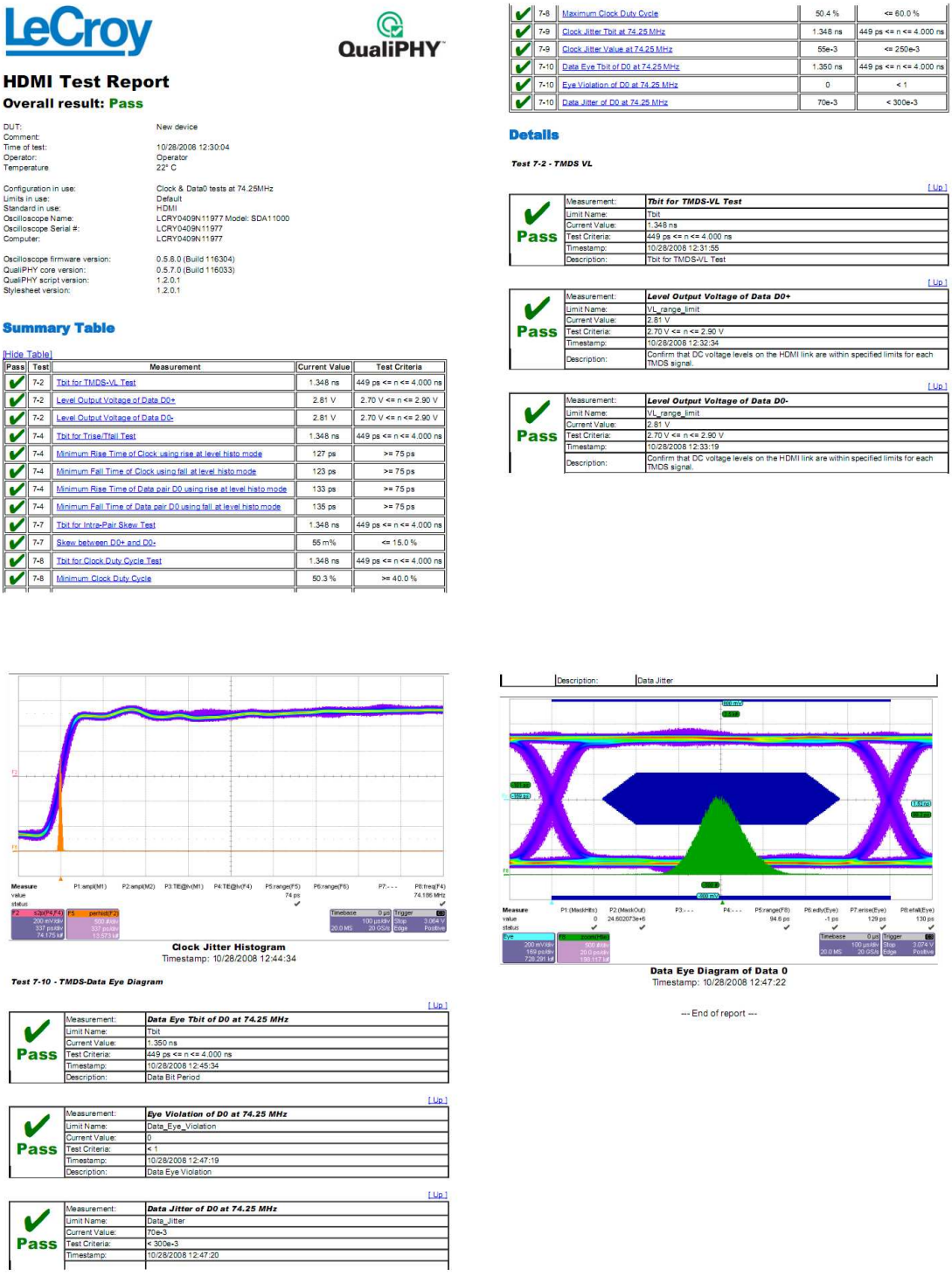


Figure 1. Report menu in QualiPHY General Setup

See the **QualiPHY Operator's Manual** for more information on how to use the QualiPHY framework.



LeCroy

QualiPHY

HDMI Test Report

Overall result: Pass

DUT:	New device
Comment:	
Time of test:	10/28/2008 12:30:04
Operator:	Operator
Temperature	22° C
Configuration in use:	Clock & Data0 tests at 74.25MHz
Limits in use:	Default
Standard in use:	HDMI
Oscilloscope Name:	LCRY0409N11977,Model: SDA11000
Oscilloscope Serial #:	LCRY0409N11977
Computer:	LCRY0409N11977
Oscilloscope firmware version:	0.5.8.0 (Build 116304)
QualiPHY core version:	0.5.7.0 (Build 116033)
QualiPHY script version:	1.2.0.1
Stylesheet version:	1.2.0.1

Summary Table

[Hide Table]

Pass	Test	Measurement	Current Value	Test Criteria
✔	7-2	Tbit for TMDS-VL Test	1.348 ns	449 ps <= n <= 4.000 ns
✔	7-2	Level Output Voltage of Data D0+	2.81 V	2.70 V <= n <= 2.90 V
✔	7-2	Level Output Voltage of Data D0-	2.81 V	2.70 V <= n <= 2.90 V
✔	7-4	Tbit for Trise/Tfall Test	1.348 ns	449 ps <= n <= 4.000 ns
✔	7-4	Minimum Rise Time of Clock using rise at level histo mode	127 ps	>= 75 ps
✔	7-4	Minimum Fall Time of Clock using fall at level histo mode	123 ps	>= 75 ps
✔	7-4	Minimum Rise Time of Data pair D0 using rise at level histo mode	133 ps	>= 75 ps
✔	7-4	Minimum Fall Time of Data pair D0 using fall at level histo mode	135 ps	>= 75 ps
✔	7-7	Tbit for Intra-Pair Skew Test	1.348 ns	449 ps <= n <= 4.000 ns
✔	7-7	Skew between D0+ and D0-	55 m%	<= 15.0 %
✔	7-8	Tbit for Clock Duty Cycle Test	1.348 ns	449 ps <= n <= 4.000 ns
✔	7-8	Minimum Clock Duty Cycle	50.3 %	>= 40.0 %
✔	7-8	Maximum Clock Duty Cycle	50.4 %	<= 60.0 %
✔	7-9	Clock Jitter Tbit at 74.25 MHz	1.348 ns	449 ps <= n <= 4.000 ns
✔	7-9	Clock Jitter Value at 74.25 MHz	55e-3	<= 250e-3
✔	7-10	Data Eye Tbit of D0 at 74.25 MHz	1.350 ns	449 ps <= n <= 4.000 ns
✔	7-10	Eye Violation of D0 at 74.25 MHz	0	< 1
✔	7-10	Data Jitter of D0 at 74.25 MHz	70e-3	< 300e-3

Details

Test 7-2 - TMDS VL

[Up]

Pass		
	Measurement:	***Tbit for TMDS-VL Test***
	Limit Name:	Tbit
	Current Value:	1.348 ns
	Test Criteria:	449 ps <= n <= 4.000 ns
	Timestamp:	10/28/2008 12:31:55
	Description:	Tbit for TMDS-VL Test

[Up]

Pass		
	Measurement:	***Level Output Voltage of Data D0+***
	Limit Name:	VL_range_limit
	Current Value:	2.81 V
	Test Criteria:	2.70 V <= n <= 2.90 V
	Timestamp:	10/28/2008 12:32:34
	Description:	Confirm that DC voltage levels on the HDMI link are within specified limits for each TMDS signal.

[Up]

Pass		
	Measurement:	***Level Output Voltage of Data D0-***
	Limit Name:	VL_range_limit
	Current Value:	2.81 V
	Test Criteria:	2.70 V <= n <= 2.90 V
	Timestamp:	10/28/2008 12:33:19
	Description:	Confirm that DC voltage levels on the HDMI link are within specified limits for each TMDS signal.

Clock Jitter Histogram
Timestamp: 10/28/2008 12:44:34

Test 7-10 - TMDS-Data Eye Diagram

[Up]

Pass		
	Measurement:	***Data Eye Tbit of D0 at 74.25 MHz***
	Limit Name:	Tbit
	Current Value:	1.350 ns
	Test Criteria:	449 ps <= n <= 4.000 ns
	Timestamp:	10/28/2008 12:45:34
	Description:	Data Bit Period

[Up]

Pass		
	Measurement:	***Eye Violation of D0 at 74.25 MHz***
	Limit Name:	Data_Eye_Violation
	Current Value:	0
	Test Criteria:	< 1
	Timestamp:	10/28/2008 12:47:19
	Description:	Data Eye Violation

[Up]

Pass		
	Measurement:	***Data Jitter of D0 at 74.25 MHz***
	Limit Name:	Data_Jitter
	Current Value:	70e-3
	Test Criteria:	< 300e-3
	Timestamp:	10/28/2008 12:47:20

Description: Data Jitter

Data Eye Diagram of Data 0
Timestamp: 10/28/2008 12:47:22

--- End of report ---

Figure 2. The Test Report includes a summary table with links to the detailed test results

Oscilloscope Option Key Installation

An option key must be purchased to enable the QPHY-HDMI option. Call LeCroy Customer Support to place an order and receive the code.

Enter the key and enable the purchased option as follows:

1. From the oscilloscope menu select **Utilities →Utilities Setup...**
2. Select the **Options** tab and click the **Add Key** button.
3. Enter the **Key Code** using the on-screen keyboard.
4. Restart the oscilloscope to activate the option after installation.

Typical (Recommended) Configuration

QualiPHY software can be executed from the oscilloscope or a host computer. The first step is to install QualiPHY. Please refer to the QualiPHY Operator's Manual for installation instructions.

LeCroy recommends running QualiPHY on an oscilloscope equipped with Dual Monitor Display capability (Option DMD-1 for oscilloscopes where this is not standard). This allows the waveform and measurements to be shown on the oscilloscope LCD display while the QualiPHY application and test results are displayed on a second monitor.

By default, the oscilloscope appears as a local host when QualiPHY is executed in the oscilloscope. Follow the steps under **Oscilloscope Selection** (as follows) and check that the IP address is 127.0.0.1.

Remote (Network) Configuration

It is also possible to install and run QualiPHY on a host computer, controlling the oscilloscope with a Network/LAN Connection.

The oscilloscope must already be configured, and an IP address (fixed or network-assigned) must already be established.

Oscilloscope Selection

Set up the oscilloscope using QualiPHY over a LAN (Local Area Network) by doing the following:

1. Make sure the host computer is connected to the same LAN as the oscilloscope. If unsure, contact your system administrator.
2. From the oscilloscope menu, select **Utilities → Utilities Setup…**
3. Select the **Remote** tab.
4. Verify the oscilloscope has an IP address and the control is set to TCP/IP.
5. Run QualiPHY in the host computer and click the **General Setup** button.
6. Select the **Connection** tab.
7. Enter the IP address from step 4 (previous).
8. Click the **Close** button.

QualiPHY is now ready to control the oscilloscope.

QualiPHY tests the oscilloscope connection after clicking the **Start** button. The system prompts you if there is a connection problem. QualiPHY's **Scope Selector** function can also be used to verify the connection. Please refer to the **QualiPHY Operator's Manual** for explanations on how to use Scope Selector and other QualiPHY functions.

Accessing the QPHY-HDMI Software using QualiPHY

This topic provides a basic overview of QualiPHY's capabilities. Please refer to the **QualiPHY Operator's Manual** for detailed information.

Access the QPHY-PCIe software using the following steps:

1. Wait for the oscilloscope to start and have its main application running.
2. Launch QualiPHY from the **Analysis** menu if installed on the oscilloscope or from the desktop icon if installed on a host computer.
3. From the QualiPHY main window (as follows), select **Standard**, then **HDMI** from the pop-up menu (if not already selected). If you check the **Pause on Failure** box (circled) QualiPHY prompts to retry the measure whenever a test fails.

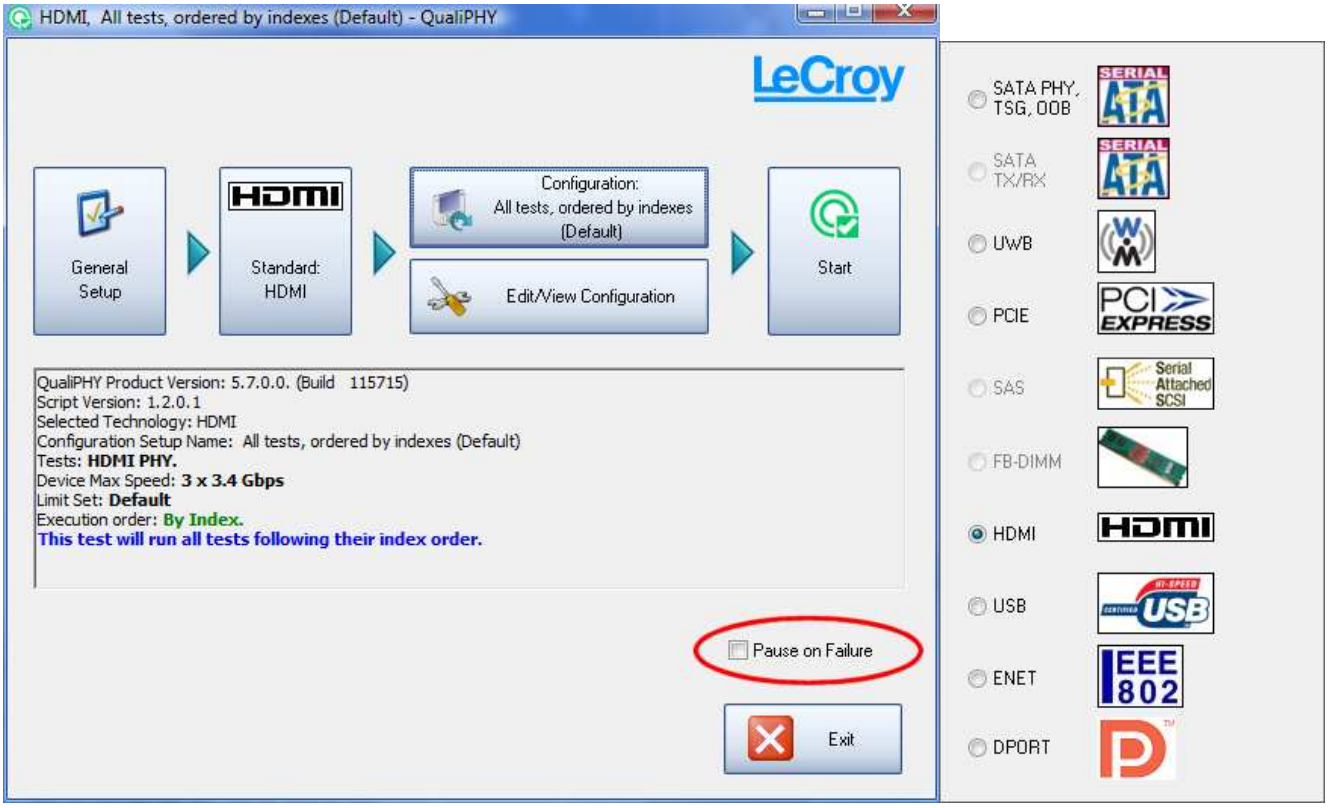
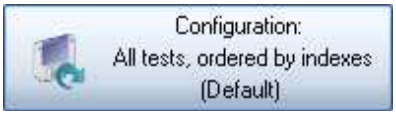


Figure 3. QualiPHY main menu and compliance test Standard selection menu

4. Click the **Configuration** button in the QualiPHY main menu:



5. Select a configuration from the pop-up menu:

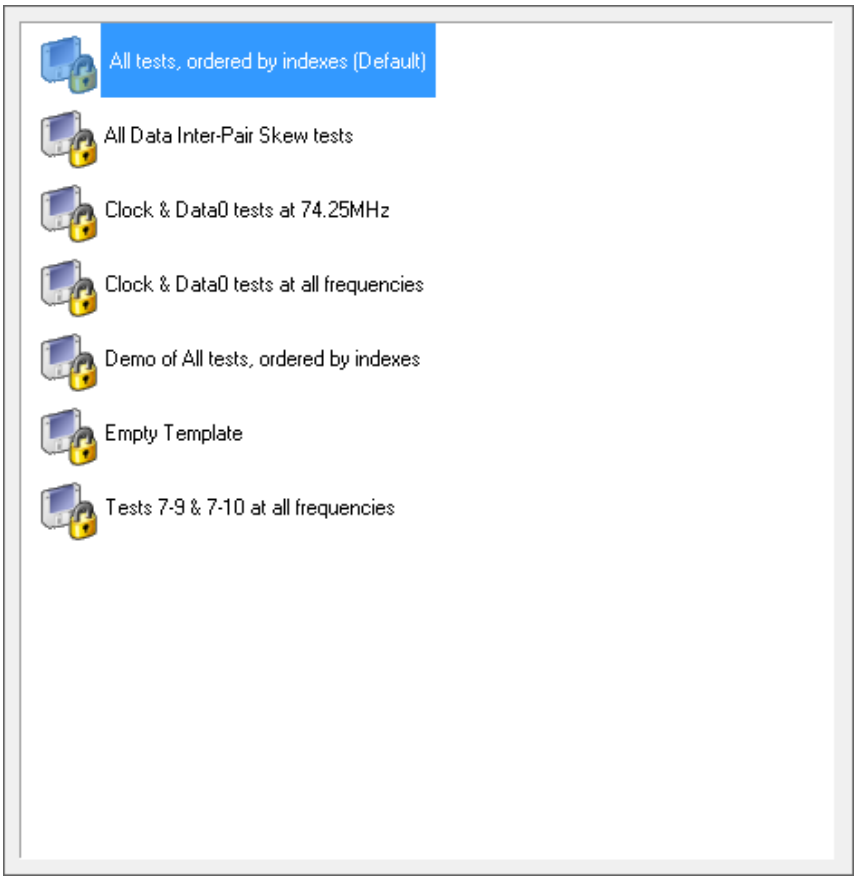


Figure 4. QualiPHY configuration selection menu

6. Click **Start**.

7. Follow the pop-up window prompts.

Customizing QualiPHY

The predefined configurations in the **Configuration** screen cannot be modified. However, you can create your own test configurations by copying one of the standard test configurations and making modifications. A description of the test is also shown in the description field when selected.

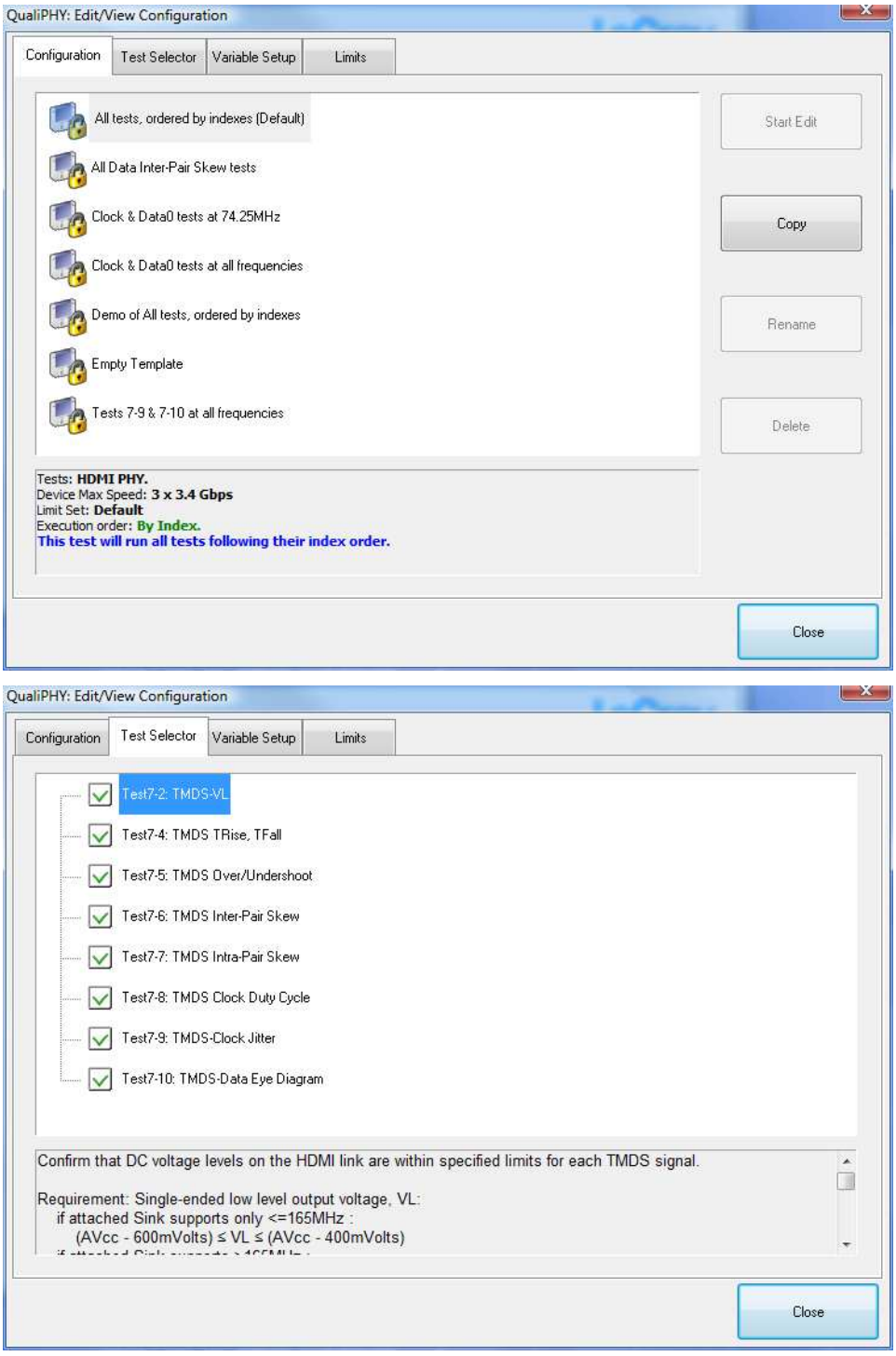


Figure 5. QualiPHY test item selection menu

Once a custom configuration is defined, script variables and the test limits can be changed by using the **Variable Setup** and **Limits Manager** from the **Edit/View Configuration** window.

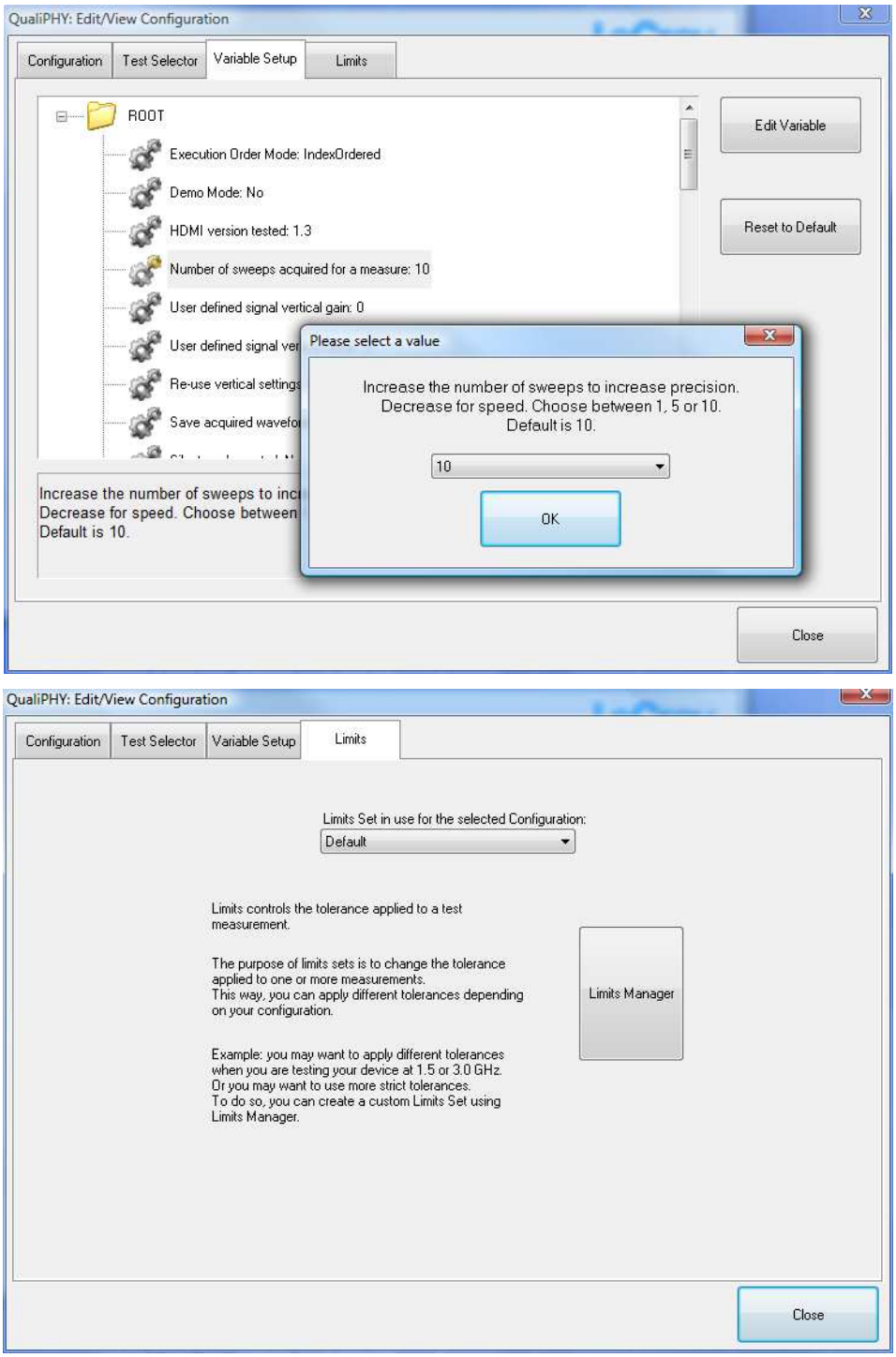


Figure 6. Variable Setup and Limits Manager windows

QPHY-HDMI Operation

After pressing **Start** in the QualiPHY menu, the software instructs how to set up the test using pop-up connection diagrams and dialog boxes.

Figure 7. Start button

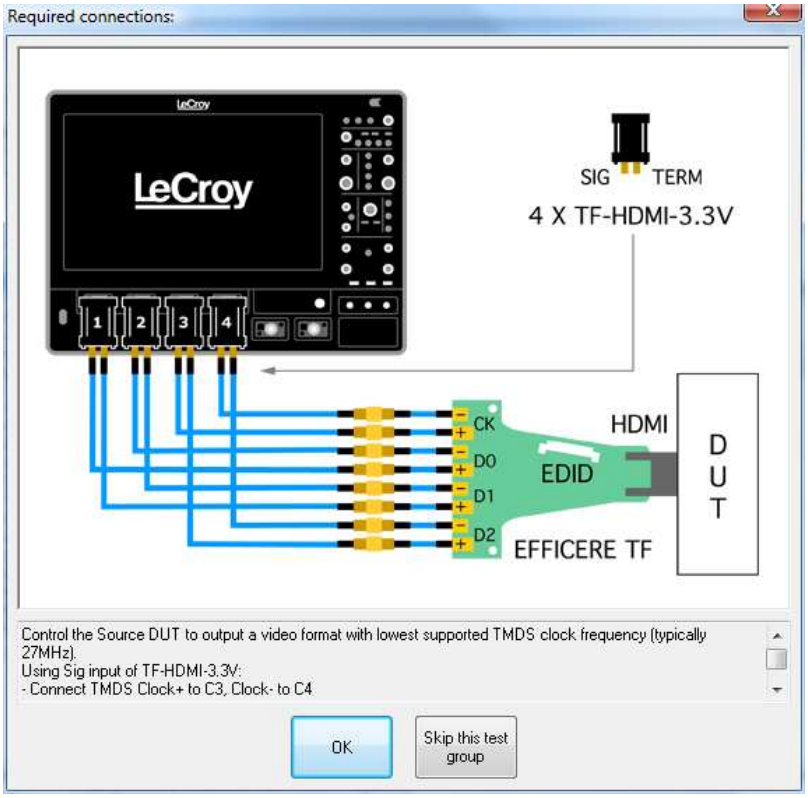


Figure 8. Example of pop-up connection diagram and dialog box

HDMI MEASUREMENT PREPARATION

SMA probing solution

LeCroy direct measurement solution uses SMA cables to connect 2 differential signals at a time to the oscilloscope channels through the TF-HDMI-3.3V SIG input. SMA cables are also used to terminate the unused signal onto specific TERM inputs.

Before beginning any test or data acquisition, the oscilloscope must be warmed for at least 20 minutes. Calibration is automatic under software control and no manual calibration is required. This procedure should be run again if the temperature of the oscilloscope changes by more than a few degrees.

Channel Deskew using Oscilloscope Calibrator Output (SMA Cables)

HDMI signals are properly probed using two separate channels on the oscilloscope connected to the appropriate SMA jacks on the test fixture. The highest measurement accuracy is achieved when the timing skew between the two channels is calibrated. This is performed using the **Deskew** control on one of the two channels to which the differential signal is connected, as follows:

1. Attach the calibrator signal to both input channels using a T connector or resistive divider to route the calibrator signal on the SDA front panel through the same cables that will be connected to the fixture. The calibrator peak voltage should be set to the same value as the nominal voltage of D^+ and D^-.

Note: This procedure demonstrates how to deskew channels 2 and 3. For optimal results, this method should be followed for channels 2 and 3, and then channels 1 and 2, followed by channels 4 and 3 to insure that all channels are deskew appropriately.

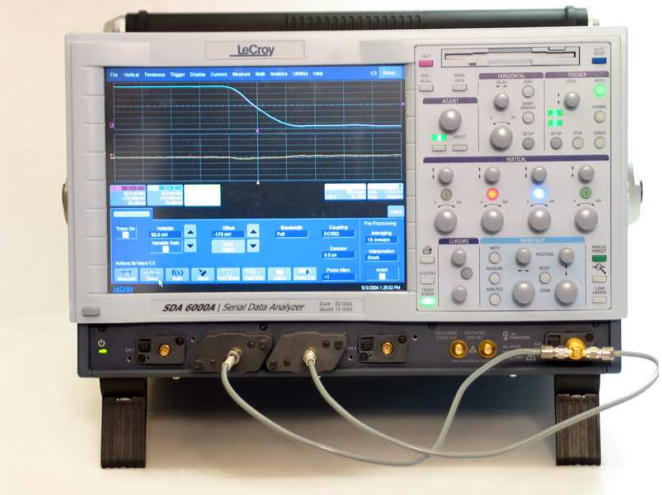


Figure 9. Deskew cable setup

2. Set interpolation of both channels to **Sin(x)/x**, using the **Interpolation** control in the **Vertical Adjust** dialog for each channel.
3. Check the **Invert** checkbox on one channel.

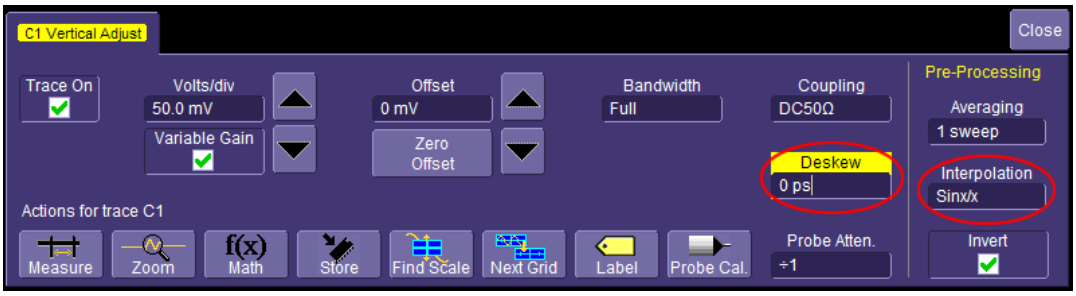


Figure 10. Deskew control in channel menu: adjust this value to achieve minimum skew

4. Create a Difference math waveform by selecting **Math → Math Setup…** from the menu bar.

   Touch the **Operator1** field and select **Difference** from the **Select Math Operator** menu.

   Enter the channels to which your signal is connected in the **Source1** and **Source2** fields. The math function is thus defined as the difference between the 2 channels probing the D^+ and D^- signals.

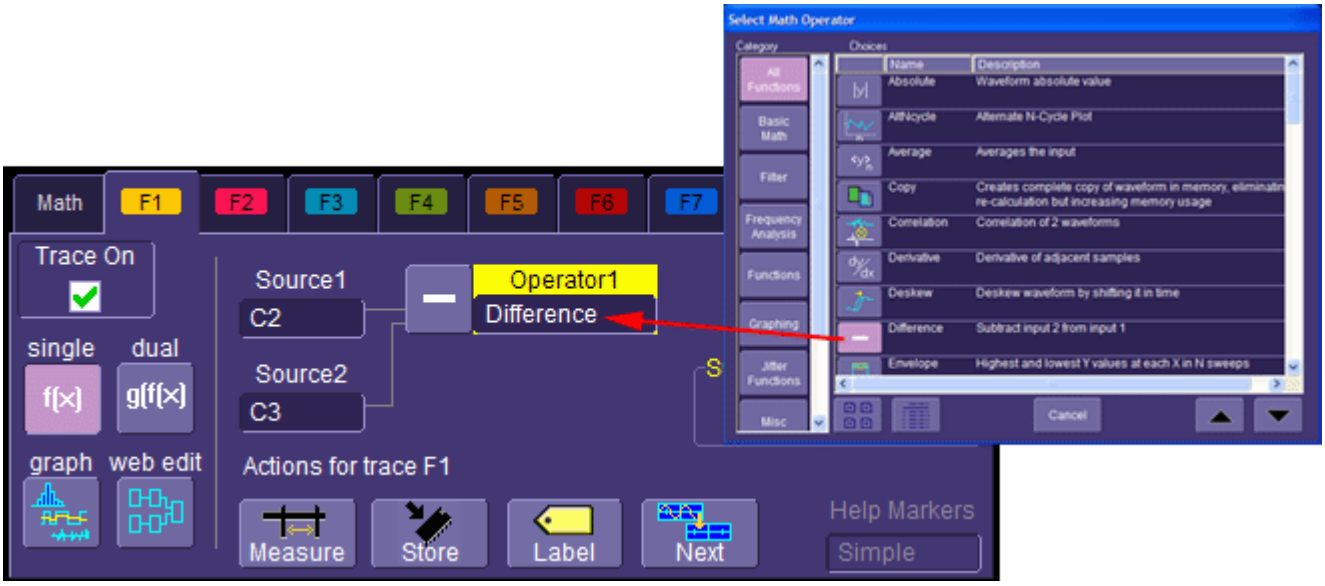


Figure 11. Math setup

5. While viewing the math trace, adjust the **Deskew** control in one of the channels until the math trace is as flat as possible.

Note: With the **Deskew** control highlighted, you can use the front panel adjust knob to make the adjustment.

The best accuracy is achieved by setting the level of the calibrator signal to match the expected levels of the signal under test, and with the calibrator set to its maximum frequency (5 MHz). The calibrator settings can be found in **Utilities → Aux Output**.

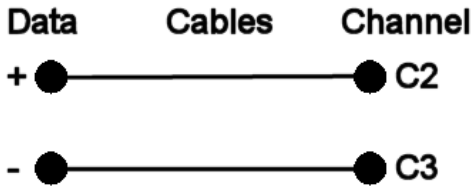
Channel Deskew using Device Under Test Signal (SMA Cables with the TF-HDMI-3.3V)

This is a multi-step procedure which is more complicated than the procedure given above. Its advantages are:

- No adapters needed.
- De-skew at the same V/div settings you'll use to capture your data (because you are capturing your data for this procedure)
- If the differential data signal has higher speed edges than the oscilloscope's AUX OUT, it is easier to get good timing measurements with the faster edges. This is definitely the case for HDMI.

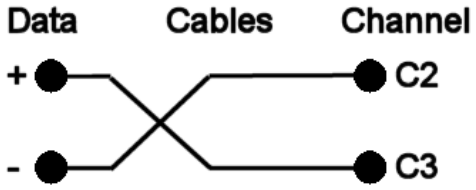
Here is the step by step procedure:

1. Connect a differential data signal to C2 and C3 using two approximately matching cables. Set up the oscilloscope as you plan to use it. Set the timebase to capture a few repetitions of the compliance test pattern (at least a few dozen edges). Press **Auto**, so the oscilloscope acquires.



Note: This procedure demonstrates how to deskew channels 2 and 3. For optimal results, this method should be followed for channels 2 and 3, and then channels 1 and 2, followed by channels 4 and 3 to insure that all channels are deskew appropriately.

2. On the C3 menu, check **Invert**. Now C2 and C3 should look the same.
3. Using the **Measure Setup**, set P1 to measure the Skew of C2, C3. Turn on **Statistics** (**Measure** menu). Write down the mean skew value after it stabilizes. This mean skew value is the addition of Data skew + cable skew + channel skew.
4. Swap the cable connections on the Data source side (on the test fixture), and then press the **Clear Sweeps** button on the oscilloscope (to clear the accumulated statistics; since we changed the input).



5. Write down the mean skew value after it stabilizes. This mean skew value is the addition of (-Data skew) + cable skew + channel skew.
6. Add the two mean skew values and divide the sum in half:

$$\frac{[\text{Data skew} + \text{cable skew} + \text{channel skew}] + [\ (-\text{Data skew}) + \text{cable skew} + \text{channel skew}]}{2}$$

7. The above formula simplifies to:

$$[\text{cable skew} + \text{channel skew}]$$

8. Set the resulting value as the **Deskew** value in C2 menu.
9. Restore the cable connections to their Step 1 settings (previous). Press the **Clear Sweeps** button on the oscilloscope. The mean skew value should be approximately zero - that is the data skew. Typically, results are <1ps given a test fixture meant to minimize skew on the differential pair.

10. On the C3 menu, un-check the **Invert** checkbox and turn off the parameters.

Now the oscilloscope inter-channel skew and cable skew is compensated for, you are ready to test.

The procedure as given above relies on the default setup of the Skew parameter (which is: detecting positive edges on both signals, at 50%). C3 was inverted in order to make C2 and C3 both have positive edges at the same time. The default setup of any parameter is in effect at the time it is set up.

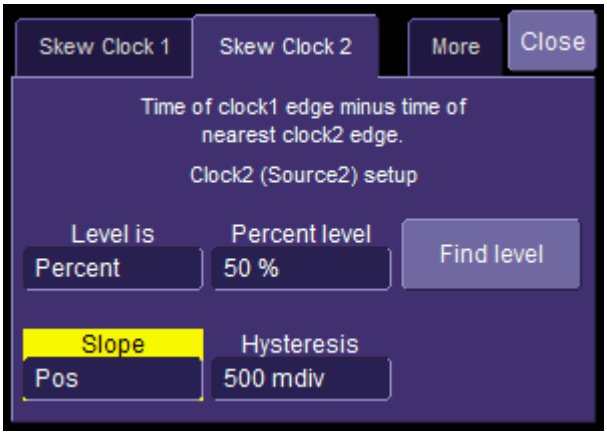


Figure 12. The Skew parameter right side dialog, Skew Clock 2 tab, showing default setup

Figure 13. Signals properly adjusted for best accuracy

Note: The signal levels should be adjusted in the Vertical Adjust dialog so at least 6 vertical divisions are filled.

QPHY-HDMI TEST CONFIGURATIONS

Configurations include variable settings and limit sets as well, not just test selections. See the QPHY-HDMI Variables section for a description of each variable value and its default value. There is only one limit sets for QPHY-HDMI.

All tests, ordered by indexes (Default)

Tests: **HDMI PHY.**
Device Max Speed: **3 x 3.4 Gbps**
Limit Set: **Default**
Execution order: **By Index.**
This test will run all tests following their index order.

All Data Inter-Pair Skew tests

Tests: **HDMI PHY.**
Device Max Speed: **3 x 3.4 Gbps**
Limit Set: **Default**
This test will run Data Inter Pair Skew for all Data signal.

Clock & Data0 tests at 74.25MHz

Tests: **HDMI PHY.**
Device Max Speed: **3 x 3.4 Gbps**
Limit Set: **Default**
This test will run all tests which can be done on Clock and Data0 (that is without changing cable connections).

Clock & Data0 tests at all frequencies

Tests: **HDMI PHY.**
Device Max Speed: **3 x 3.4 Gbps**
Limit Set: **Default**
This test will run all tests which can be done on Clock and Data0 (that is without changing cable connections).

Demo of All tests, ordered by indexes

Tests: **HDMI PHY.**
Device Max Speed: **3 x 3.4 Gbps**
Limit Set: **Default**
Execution order: **By Index.**
This test will run a Demo of all tests following their index order (this will use stored waveforms).

Empty Template

Tests: **HDMI PHY.**
Device Max Speed: **3 x 3.4 Gbps**
Limit Set: **Default**
No tests selected, copy this template to construct a custom configuration

Tests 7-9 & 7-10 at all frequencies

Tests: **HDMI PHY.**
Device Max Speed: **3 x 3.4 Gbps**
Limit Set: **Default**
This test will run test Jitter and Eye Diagram tests for all frequencies.

QPHY-HDMI VARIABLES

Execution Order Mode

Choose between CablingOrdered and IndeOrdered to define how the tests will be run. Currently only IndexOrdered is available.

Demo Mode

Select demonstration mode. When enabled, previously stored HDMI waveforms will be used.

HDMI version tested

Select HDMI Compliance test version. There are two versions available: 1.0 and 1.3. Currently only 1.3 is available.

Number of sweeps acquired for a measure

Increase the number of sweeps to increase precision. Decrease for speed. Choose between 1, 5 or 10. Default is 10.

User defined signal vertical gain

Default is 0.

If set to default (or negative value), the script will initiate an automated find scale to determine the gain and offset.

If set to a positive value, it will be used to set the gain of all signals and the "Re-use vertical settings" variable will be ignored.

User defined signal vertical offset

If a "User defined signal vertical gain" is defined (> 0), this offset will be used for the signal and trigger levels.

Re-use vertical settings

Enable re-use of memorized vertical settings (to speed up test). Choose between Yes and No.

Default is No (disabled) to ensure gain and offset are correctly set.

This variable is ignored if "User defined signal vertical gain" > 0.

Save acquired waveforms

Saved waveforms can be used later in demonstration or optimized version of script.

Choose between Yes or No. Default is No.

This setting is ignored (no save) if using stored waveforms is enabled and in Demo mode.

Silent mode control

No more interaction with the user when silent mode is on. Choose between Yes or No. Default is No.

Useful to let the test run repetitively in the background.

TMDS Data Pair to test

Define which Data Pair to test. Connect TMDS DATA + to C1 and DATA - to C2.

Choose between D0, D1, D2 or D1,D2,D3. The last option is the default and will test all Data Pairs.

Use stored trace for pixel clock measure

Optimization to measure only once the pixel clock frequency. Choose between Yes and No, Default is No.

Waveform Path

Specify the path on the oscilloscope to save/recall waveforms. When not in Demo Mode and Save acquired waveforms is enabled, the waveforms will be saved in this folder. When set to Demo Mode or Use stored trace for pixel clock measure, saved waveforms should be available in this folder. Default is "D:\Waveforms\HDMI".

Test7-2: TMDS-VL

Number of segments acquired in sequence

HDMI specification requires 10'000 segments.

For debugging only, reduce the number of segments to speed-up processing. Choose between 10’000, 1000, 500 or 50. Default is 10’000.

Recalled Waveform File Index (5 digits)

Enter the 5 digits number corresponding to the index of the file you want to recall. Default is 00000.

Support of TMDS frequency >= 165 MHz

Choose between Yes or No. Default is No.

If attached Sink device supports only <=165MHz, limit is: (AVcc - 600mVolts) ≤ VL ≤ (AVcc - 400mVolts)

If attached Sink device supports >165MHz, limit is: (AVcc - 700mVolts) ≤ VL ≤ (AVcc - 400mVolts)

Test7-4: TMDS TRise, TFall

Recalled Waveform File Index (5 digits)

Enter the 5 digits number corresponding to the index of the file you want to recall. Default is 00000.

Use internal peak if signal has two peaks

Default is No. Choose Yes to debug specific signal shape.

HDMI signals can have two peaks in amplitude. Classic measure of rise/fall time at 20-80% doesn't give stable results in this case. So if two peaks are detected, we can use the internal one to determine rise/fall levels.

But we have observed signals with "faked" internal peaks. These additional peaks give inaccurate (too short) rise/fall time. So disabling the use of internal peaks allows forcing usage of the highest peaks.

Test7-6: TMDS Inter-Pair Skew

Data-Data test combinations

Choose the combination of Data Pair to be tested between D0-D2 or D0-D1 or D2-D1 or D0-D2,D0-D1,D2-D1. The last option is the default and will test all Data Pairs.

Recalled Waveform File Index (5 digits)

Enter the 5 digits number corresponding to the index of the file you want to recall. Default is 00000.

Test7-7: TMDS Intra-Pair Skew

Number of segments acquired in sequence

HDMI specification requires 10'000 segments.

For debugging only, reduce the number of segments to speed-up processing. Choose between 10’000, 1000, 500 or 50. Default is 10’000.

Recalled Waveform File Index (5 digits)

Enter the 5 digits number corresponding to the index of the file you want to recall. Default is 00000.

Test7-8: TMDS Clock Duty Cycle

Number of segments acquired in sequence

HDMI specification requires 10'000 segments.

For debugging only, reduce the number of segments to speed-up processing. Choose between 10’000, 1000, 500 or 50. Default is 10’000.

Recalled Waveform File Index (5 digits)

Enter the 5 digits number corresponding to the index of the file you want to recall. Default is 00000.

Test7-9: TMDS-Clock Jitter

DUT TMDS Clock Frequencies

Configure Source DUT to output one video format for each of the following TMDS Clock frequencies if that frequency is supported by the DUT: 27MHz (or 25MHz), 74.25MHz, 148.5MHz, 222.75MHz and, if not already covered, the highest DUT-supported frequency.

Timebase used to create Eye Diagram

Increase/decrease the number of points acquired to create Eye Diagram.

100us/div gives enough samples to fulfill the 16 MS/Channel HDMI requirement.

Recalled Waveform File Index (5 digits)

Enter the 5 digits number corresponding to the index of the file you want to recall. Default is 00000.

Test7-10: TMDS-Data Eye Diagram

DUT TMDS Clock Frequencies

Configure Source DUT to output one video format for each of the following TMDS Clock frequencies if that frequency is supported by the DUT: 27MHz (or 25MHz), 74.25MHz, 148.5MHz, 222.75MHz and, if not already covered, the highest DUT-supported frequency.

Timebase used to create Eye Diagram

Increase/decrease the number of points acquired to create Eye Diagram.

100us/div gives enough samples to fulfill the 16 MS/Channel HDMI requirement.

Recalled Waveform File Index (5 digits)

Enter the 5 digits number corresponding to the index of the file you want to recall. Default is 00000.

Maximum DUT Pixel Clock Frequency

If different than 0, this value will be used as the maximum frequency in place of the standard reference for test 7-10 Eye Diagram. The frequency must be entered in scientific format, e.g. 340MHz as 340e6. Default value is 0.

QPHY-HDMI LIMIT SETS

Default

There is only one set which corresponds to the HDMI standard specification limits.

QPHY-HDMI TESTS

Test7-2: TMDS-VL

Confirm that DC voltage levels on the HDMI link are within specified limits for each TMDS signal.

Requirement: Single-ended low level output voltage, VL:

if attached Sink supports only <=165MHz :

(AVcc - 600mVolts) ≤ VL ≤ (AVcc - 400mVolts)

if attached Sink supports >165MHz :

(AVcc - 700mVolts) ≤ VL ≤ (AVcc - 400mVolts)

Reference: [HDMI: Table 4-15] Source DC Characteristics at TP1

Required Test Method

Setup:

1) Connect TPA-P adapter to Source DUT HDMI output connector.

2) Connect probe to TMDS_DATA0+. If using a differential probe, follow the manufacturer's instructions for use in measuring a single-ended signal.

3) Configure the EDID to indicate only 27MHz formats (480p and 576p, no Deep Color support) with the 640x480p Established Timings bit set.

4) Control the Source DUT to output a video format with lowest supported TMDS clock frequency (typically 27MHz).

Measure:

5) Capture 1000 or more repetitions, triggered at the vertical mid-point of the High-to-Low transition of a H-L-L-L bit sequence. Each capture must be of duration 3*TBIT.

6) Display the voltage (vertical) histogram on the scope, with the histogram data accumulated only from the last 2-bits of the H-L-L-L sequence.

7) Read the VL value as the most common low-level voltage shown on the histogram.

8) If (VL > 2.90V) OR (VL < 2.70V) then

9) Capture 10,000 repetitions, triggered at mid-point of waveform, of duration ≥ 2*TBIT to get proper histograms.

10) Display the voltage (vertical) histogram on the scope.

11) If (VL > 2.90V) OR (VL < 2.70V) then FAIL

12) Repeat the test for all eight TMDS signals.

13) If CDF field Source_Above_165 then:

14) Switch to an EDID that additionally indicates:

- Support for 1080p50Hz and 60Hz

- Deep Color 36-bits/pixel
- Max_TMDS_Clock of 225MHz (value = 225/5 = 45).

15) Repeat test sequence above still using lowest clock rate format.

16) If (VL > 2.90V) OR (VL < 2.60V) then FAIL

17) Repeat the test for all eight TMDS signals.

Test7-4: TMDS TRise, TFall

Confirm that the rise times and fall times on the TMDS differential signals fall within the limits of the specification.

Requirement: 75psec ≤ Rise Time or Fall Time

Reference: [HDMI: Table 4-16] Source AC Characteristics at TP1

Required Test Method

1) Connect TPA-P adapter to Source DUT HDMI output connector.

2) Configure Source DUT to output a video format and pixel size with highest supported TMDS clock frequency.

3) Accumulate at least 10,000 triggered waveforms.

4) Measure TRISE as the mode of the sampled edge times from 20% to 80% of the differential swing voltage rising edge.

5) Measure TFALL as the mode of the sampled edge times from 80% to 20% of the differential swing voltage on the falling edge.

6) If (TRISE < 75ps) then FAIL.

7) If (TFALL < 75ps) then FAIL.

8) Repeat the test for all remaining TMDS clock and data pairs.

Test7-5: TMDS Over/Undershoot

Confirm that the differential TMDS signals do not have overshoot or undershoot beyond that allowed by the specified limits (HDMI 1.0 only).

Test7-6: TMDS Inter-Pair Skew

Confirm that any skew within any one differential pair in the TMDS portion of the HDMI link does not exceed the limits in the specification.

Requirement: Intra-pair skew between TMDS DATA pairs must not exceed 0.15*TBIT.

Reference: [HDMI: Table 4-16] Source AC Characteristics at TP1

Required Test Method

1) Connect TPA-P adapter to the Source DUT HDMI output connector.
2) Connect first single-ended probe to TMDS_DATA0+.
3) Connect second single-ended probe to TMDS_DATA0-.
4) Configure Source DUT to output a video format and pixel size with highest supported TMDS clock frequency.
5) Set the trigger on TMDS_DATA0+ rising edge.
6) Display the waveform of TMDS_DATA0+ and DATA0-. Accumulate 10,000 or more triggers.

Find the closest falling edge of DATA0- (either preceding or following DATA0+ rising edge), and determine the most common 50% crossing point of that TMDS_DATA0- falling edge using a horizontal (time) Histogram method.

7) Measure skew from trigger point to most common 50% crossing point of TMDS_DATA0-.
8) If (skew > 0.15*TBIT) then FAIL.
9) Repeat the test for all remaining TMDS differential pairs.

Test7-7: TMDS Intra-Pair Skew

Confirm that any skew within any one differential pair in the TMDS portion of the HDMI link does not exceed the limits in the specification.

Requirement: Intra-pair skew between TMDS DATA pairs must not exceed 0.15*TBIT.

Reference: [HDMI: Table 4-16] Source AC Characteristics at TP1

Required Test Method

1) Connect TPA-P adapter to the Source DUT HDMI output connector.
2) Connect first single-ended probe to TMDS_DATA0+.
3) Connect second single-ended probe to TMDS_DATA0-.
4) Configure Source DUT to output a video format and pixel size with highest supported TMDS clock frequency.
5) Set the trigger on TMDS_DATA0+ rising edge.
6) Display the waveform of TMDS_DATA0+ and DATA0-. Accumulate 10,000 or more triggers.

Find the closest falling edge of DATA0- (either preceding or following DATA0+ rising edge), and determine the most common 50% crossing point of that TMDS_DATA0- falling edge using a horizontal (time) Histogram method.

7) Measure skew from trigger point to most common 50% crossing point of TMDS_DATA0-.

8) If (skew > 0.15*TBIT) then FAIL.

9) Repeat the test for all remaining TMDS differential pairs.

Test7-8: TMDS Clock Duty Cycle

Confirm that the TMDS Clock does not carry excessive jitter.

Requirement: TMDS differential clock jitter must not exceed 0.25*TBIT, relative to the ideal Recovery Clock.

Reference: [HDMI: Table 4-16] Source AC Characteristics at TP1

Required Test Method

1) Connect TPA-P adapter to the Source DUT HDMI output connector.

2) Connect differential probe to TMDS Clock pair.

3) Configure oscilloscope and CRU:

- Evaluate 16M samples per channel (can be acquired with a single or with multiple smaller captures).

4) Configure Source DUT to output one video format for each of the following TMDS Clock frequencies if that frequency is supported by the DUT: 27MHz (or 25MHz), 74.25MHz, 148.5MHz, and 222.75MHz. For each of these test frequencies, perform the following

• Capture the waveform and process it with the Digital Oscilloscope

ƒ If test frequency is <=165MHz then set Sampling Rate ≥10GSa/s

If test frequency is >165MHz then set Sampling Rate ≥20GSa/s

• Measure Clock jitter as difference between farthest left sampling point and farthest right sampling point, within the measurement box below:

- Vertical setting = VC = 0V ± 20mV.

• If Clock jitter exceeds 0.25*TBIT then FAIL

5) Repeat the test for remaining supported test frequencies. Only one video format/pixel-size combination is required per TMDS clock rate.

Test7-9: TMDS-Clock Jitter

Confirm that the TMDS Clock does not carry excessive jitter.

Requirement: TMDS differential clock jitter must not exceed 0.25*TBIT, relative to the ideal Recovery Clock.

Reference: [HDMI: Table 4-16] Source AC Characteristics at TP1

Required Test Method

1) Connect TPA-P adapter to the Source DUT HDMI output connector.

2) Connect differential probe to TMDS Clock pair.

3) Configure oscilloscope and CRU:

- Evaluate 16M samples per channel (can be acquired with a single or with multiple smaller captures).

4) Configure Source DUT to output one video format for each of the following TMDS Clock frequencies if that frequency is supported by the DUT: 27MHz (or 25MHz), 74.25MHz, 148.5MHz, and 222.75MHz. For each of these test frequencies, perform the following

• Capture the waveform and process it with the Digital Oscilloscope

If test frequency is <=165MHz then set Sampling Rate ≥10GSa/s

If test frequency is >165MHz then set Sampling Rate ≥20GSa/s

• Measure Clock jitter as difference between farthest left sampling point and farthest right sampling point, within the measurement box below:

- Vertical setting = VC = 0V ± 20mV.

• If Clock jitter exceeds 0.25*TBIT then FAIL

5) Repeat the test for remaining supported test frequencies. Only one video format/pixel-size combination is required per TMDS clock rate.

Test7-10: TMDS-Data Eye Diagram

Confirm that the TMDS Clock does not carry excessive jitter.

Requirement: TMDS differential clock jitter must not exceed 0.25*TBIT, relative to the ideal Recovery Clock.

Reference: [HDMI: Table 4-16] Source AC Characteristics at TP1

Required Test Method

1) Connect TPA-P adapter to the Source DUT HDMI output connector.

2) Connect differential probe to TMDS Clock pair.

3) Configure oscilloscope and CRU:

- Evaluate 16M samples per channel (can be acquired with a single or with multiple smaller captures).

4) Configure Source DUT to output one video format for each of the following TMDS Clock frequencies if that frequency is supported by the DUT: 27MHz (or 25MHz), 74.25MHz, 148.5MHz, and 222.75MHz. For each of these test frequencies, perform the following

• Capture the waveform and process it with the Digital Oscilloscope

If test frequency is <=165MHz then set Sampling Rate ≥10GSa/s

If test frequency is >165MHz then set Sampling Rate ≥20GSa/s

• Measure Clock jitter as difference between farthest left sampling point and farthest right sampling point, within the measurement box below:

- Vertical setting = VC = 0V ± 20mV.

• If Clock jitter exceeds 0.25*TBIT then FAIL

5) Repeat the test for remaining supported test frequencies. Only one video format/pixel-size combination is required per TMDS clock rate.

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